

WEST

Generate Collection

L29: Entry 6 of 20

File: USPT

Oct 24, 2000

DOCUMENT-IDENTIFIER: US 6137375 A

TITLE: Loss control loop circuit for controlling the output voltage of a voltage-controlled oscillator

Abstract Text (1):

A circuit for controlling the loss of a VCO in a master-slave tuning system includes an envelope detector, an amplitude regulator, a current-mode circuit, and a low-pass filter. The envelope detector receives the VCO output voltage and provides VCO output envelope voltage, $V_{sub.ENV}$. The amplitude regulator receives $V_{sub.ENV}$ and a reference voltage, $V_{sub.REF}$, and provides a sourcing current if $V_{sub.ENV}$ is less than $V_{sub.REF}$, and draws a sinking current if $V_{sub.ENV}$ is greater than $V_{sub.REF}$. The current-mode circuit receives $V_{sub.ENV}$ and provides a control current, $I_{sub.Q}$. The low-pass filter has high DC gain for integrating the control current and the sourcing or sinking current to provide the VCO control voltage, $V_{sub.CON}$, to the VCO. The control current, $I_{sub.Q}$, is proportional to the inverse of $V_{sub.ENV}$ multiplied by the time derivative of $V_{sub.ENV}$.

Brief Summary Text (9):

In line with these assumptions, a VCO as depicted in FIG. 2A is chosen. FIG. 2A is a block diagram of a typical prior art loss control loop which includes VCO 210, rectifier 220, adder 230, and a circuit 240 having transfer function $H(s)$. VCO 210 is depicted as an ideal fixed LC-tank circuit in parallel with $G_{sub.L}$, a conductance which models the loss of the tank at the oscillation frequency, and tunable negative conductance $-G_{sub.N}$. $G_{sub.L}$ is the narrow-band equivalent loss contributed by inductor L and capacitor C. $G_{sub.N}$ is the absolute value of the negative conductance which is controlled by $V_{sub.CON}$ to tune out the loss. $G_{sub.N}$ is assumed to increase monotonically with respect to $V_{sub.CON}$. The output of VCO 210 is provided to rectifier 220. The rectified output, $V_{sub.RECT}$, is subtracted from $V_{sub.REF}$ in adder 230, and the difference is provided to circuit 240, a filter which provides gain and generates control voltage $V_{sub.CON}$ to minimize the difference between the envelope of the VCO output, $V_{sub.ENV}$, and $V_{sub.REF}$. The envelope voltage, $V_{sub.ENV}$, is the low frequency component of the rectified output, $V_{sub.RECT}$. When $V_{sub.ENV}$ is greater than $V_{sub.REF}$, $G_{sub.N}$ is made smaller to make the tank lossy and reduce the envelope voltage, $V_{sub.ENV}$. If $V_{sub.ENV}$ is less than $V_{sub.REF}$, $G_{sub.N}$ is increased, thus making Q negative and increasing the envelope voltage, $V_{sub.ENV}$.

Brief Summary Text (10):

FIG. 2B illustrates a possible breadboard circuit realization of the prior art circuit of FIG. 2A. Circuit 240 is chosen as an integrator 270. (The signs on the inputs to adder 230 are reversed because of the minus sign introduced by integrator 270.) VCO 250 is realized as a differential LC-tank circuit in parallel with negative conductance circuit 260 which uses two MOSFETs biased in the triode region to act as variable resistors. Inserting resistors $R_{sub.1}$ and $R_{sub.2}$ in series with inductor $L_{sub.V}$ reduces the Q of VCO 250 to about 10. Such a low Q is used to demonstrate the capability of the loop to control loss. Because this circuit is realized on a breadboard, the oscillation frequency of the tank circuit is low, around 3 MHz.

Brief Summary Text (14):

In accordance with the present invention, a loss control loop circuit for controlling the amplitude of the output voltage of a VCO which is controlled by a VCO control voltage includes an envelope detector which receives the VCO output voltage and provides VCO output envelope voltage, $V_{sub.ENV}$, an amplitude regulator which receives $V_{sub.ENV}$ and a reference voltage, $V_{sub.REF}$, and provides a sourcing

current if $V_{\text{sub.ENV}}$ is less than $V_{\text{sub.REF}}$, and draws a sinking current if $V_{\text{sub.ENV}}$ is greater than $V_{\text{sub.REF}}$, a current-mode circuit which receives $V_{\text{sub.ENV}}$ and provides a control current, $I_{\text{sub.Q}}$, a low-pass filter having high DC gain for integrating the control current and the sourcing or sinking current from the amplitude regulator to provide the VCO control voltage, $V_{\text{sub.CON}}$, to the VCO, and means for providing $V_{\text{sub.CON}}$ to the VCO.

Brief Summary Text (18):

The amplitude regulator includes a voltage difference detector and a charge pump. The voltage difference detector receives $V_{\text{sub.ENV}}$ and $V_{\text{sub.REF}}$ and provides an up signal if $V_{\text{sub.ENV}}$ is less than $V_{\text{sub.REF}}$ and provides a down signal if $V_{\text{sub.ENV}}$ is greater than $V_{\text{sub.REF}}$. The charge pump receives the up and down signals and provides sourcing current if the up signal is high and draws sinking current if the down signal is high.

Brief Summary Text (19):

Also provided is a loss control loop circuit for stabilizing the amplitude of the output voltage of a VCO which is controlled by a VCO control voltage which includes an envelope detector which receives the VCO output voltage and provides $V_{\text{sub.ENV}}$, a current-mode circuit which receives $V_{\text{sub.ENV}}$ and provides a control current, $I_{\text{sub.Q}}$, a low-pass filter having high DC gain for integrating the control current to provide the VCO control voltage, $V_{\text{sub.CON}}$, to the VCO, and means for providing $V_{\text{sub.CON}}$ to the VCO.

Brief Summary Text (20):

An important difference over the prior art, which included a VCO whose control voltage is provided at the output of a filter, is the inclusion of an envelope detector that generates $V_{\text{sub.ENV}}$ and an amplitude regulator and a current-mode circuit that are coupled in parallel between the output terminal of the envelope detector and the input terminal of the filter. The filter is a low-pass filter having high DC gain. The current-mode circuit converts $V_{\text{sub.ENV}}$ to a current proportional to the inverse of $V_{\text{sub.ENV}}$ multiplied by the time derivative of $V_{\text{sub.ENV}}$. It is preferable that a microwave integrated filter has its loss controlled by the loss control loop circuit of the present invention.

Brief Summary Text (21):

A master-slave filter tuning system is also provided which uses the loss control loop circuit described above as a Q-control circuit. Also included in the system are a tuned filter which receives an input voltage and provides a filtered output voltage, and which also receives a frequency control signal and a Q-control signal. The system also includes a frequency control circuit which provides the tuned filter frequency control signal, a Q-control circuit which provides the tuned filter Q-control signal, and a voltage-controlled oscillator (VCO) which receives the tuned filter frequency control signal and the tuned filter Q-control signal and provides a VCO output voltage. The Q-control circuit includes an envelope detector which receives the VCO output voltage and provides $V_{\text{sub.ENV}}$, an amplitude regulator which receives $V_{\text{sub.ENV}}$ and $V_{\text{sub.REF}}$ and provides a sourcing current if $V_{\text{sub.ENV}}$ is less than $V_{\text{sub.REF}}$, and draws a sinking current if $V_{\text{sub.ENV}}$ is greater than $V_{\text{sub.REF}}$, a current-mode circuit which receives $V_{\text{sub.ENV}}$ and provides control current $I_{\text{sub.Q}}$, and a low-pass filter having high DC gain for integrating $I_{\text{sub.Q}}$ and the sourcing or sinking current from the amplitude regulator to provide the VCO control voltage, $V_{\text{sub.CON}}$, to the VCO. The control current, $I_{\text{sub.Q}}$, is proportional to the inverse of $V_{\text{sub.ENV}}$ multiplied by the time derivative of $V_{\text{sub.ENV}}$.

Detailed Description Text (2):

The present invention provides a loss control loop circuit made up of VCO 110 and Q-control circuit 130 of FIG. 1. This loss control loop circuit controls the Q of VCO 110 while regulating the amplitude of the output of the VCO. In the prior art loss control loop circuit in FIG. 2A, which includes VCO 210, rectifier 220, voltage adder 230, and a circuit 240 having transfer function $H(s)$, the VCO output envelope voltage (low-pass-filtered output of rectifier 220) is measured in an attempt to control the Q of the VCO tank circuit. But the relation between the envelope voltage, $V_{\text{sub.ENV}}$, and Q is weak--setting the value of Q equal to infinity does not uniquely set the value of $V_{\text{sub.ENV}}$, and therefore $V_{\text{sub.ENV}}$ cannot be used as a

measurement of Q . The circuit is thus not able to adequately control the VCO output, as shown in FIG. 2C. The loss control loop circuit of the present invention uses a much better Q measurement. A current-mode circuit based on this Q measurement controls the Q of tuned system 10, and an amplitude regulator, consisting of a voltage difference detector and a charge pump, regulates the amplitude of the VCO output. The sum of the currents generated by the current-mode circuit and the amplitude regulator is integrated by a low-pass filter having high DC gain. By properly choosing the value of a capacitor in the current-mode circuit, the current sources in the charge pump, and the frequency response of the low-pass filter, $V_{sub.ENV}$ and the VCO control voltage, $V_{sub.CON}$, can both be kept within narrow limits in the steady state. $V_{sub.CON}$ is then able to be averaged or sampled and held in order to control the frequency of tuned filter 100. The Q measurement method is first described, followed by a method of determining the system parameters.

Detailed Description Text (4):

Current-mode circuit 300 includes transconductor 310, current adder 320, identical NPN bipolar transistors $Q_{sub.1}$ and $Q_{sub.2}$, identical n-channel MOSFETs $M_{sub.1}$ and $M_{sub.2}$, identical n-channel MOSFETs $M_{sub.3}$ and $M_{sub.4}$ forming DC current sources $I_{sub.0}$ controlled by $V_{sub.bias\ n1}$, frequency compensation capacitors $C_{sub.1}$ and $C_{sub.2}$, and capacitor $C_{sub.x}$. $V_{sub.ENV}$ is provided to transconductor 310, a voltage-to-current converter, which outputs two equal currents $I_{sub.ENV}$. One realization of transconductor 310 is shown in FIG. 3B. This transconductor uses NPN bipolar transistors $Q_{sub.3}$, $Q_{sub.4}$, $Q_{sub.5}$, $Q_{sub.6}$, a MOSFET current source $M_{sub.15}$ controlled by bias voltage $V_{sub.bias\ n2}$, and a high-swing current mirror made of six p-channel MOSFETs $M_{sub.9}$ - $M_{sub.14}$ and controlled by $V_{sub.bias\ p2}$. The value of $V_{sub.bias\ p2}$ is such that $M_{sub.9}$, $M_{sub.10}$, and $M_{sub.11}$ operate at the edge of the saturation region. Current-mode circuit 300 is made of two nearly identical subcircuits 311 and 312, each of which includes one of the two NPN bipolar transistors $Q_{sub.1}$, $Q_{sub.2}$, two of the n-channel MOSFETs $M_{sub.1}$ and $M_{sub.3}$, $M_{sub.2}$ and $M_{sub.4}$, and one of the frequency compensation capacitors $C_{sub.1}$, $C_{sub.2}$. The difference between the subcircuits is that subcircuit 311 also includes capacitor $C_{sub.x}$ through which a current $I_{sub.x}$ flows. Subcircuits 311 and 312 respectively generate $I_{sub.1}$ and $I_{sub.2}$, the drain currents of MOSFETs $M_{sub.1}$ and $M_{sub.2}$, respectively, both of which are provided to current adder 320. Current adder 320 is a current mirror which includes four p-channel MOSFETs, $M_{sub.5}$ - $M_{sub.8}$. The sources of $M_{sub.7}$ and $M_{sub.8}$ are connected to supply voltage $V_{sub.dd}$, typically 3V. The drains of $M_{sub.7}$ and $M_{sub.8}$ are respectively connected to the sources of $M_{sub.5}$ and $M_{sub.6}$. The gates of $M_{sub.7}$ and $M_{sub.8}$ are coupled together and to the drains of $M_{sub.6}$ and $M_{sub.2}$. The gates of $M_{sub.5}$ and $M_{sub.6}$ are coupled together and to a bias voltage $V_{sub.bias\ p1}$ which is used in a high-swing current mirror biasing scheme. Like $V_{sub.bias\ p2}$ the value of $V_{sub.bias\ p1}$ is chosen so that $M_{sub.7}$ and $M_{sub.8}$ operate at the edge of the saturation region. The drain of $M_{sub.5}$ is connected to the drain of $M_{sub.1}$, from which the output current, $I_{sub.Q}$, is taken. $I_{sub.Q}$ of current-mode circuit 300 is the difference between $I_{sub.2}$ and $I_{sub.1}$.

Detailed Description Text (5):

These two currents, $I_{sub.1}$ and $I_{sub.2}$, are generated as follows. In each subcircuit, $I_{sub.ENV}$ is provided to the collector of bipolar transistor $Q_{sub.1}$ or $Q_{sub.2}$, whose emitter is coupled to ground. The gate of MOSFET $M_{sub.1}$ or $M_{sub.2}$ is coupled to the collector of one of the bipolar transistors. The source of MOSFET $M_{sub.1}$ or $M_{sub.2}$ is coupled to the base of bipolar transistor $Q_{sub.1}$ or $Q_{sub.2}$, respectively, from which the DC current source $I_{sub.0}$ is provided to ground. The frequency compensation capacitors $C_{sub.1}$ and $C_{sub.2}$ have the same value and are connected between the gate and source of MOSFET $M_{sub.1}$ and $M_{sub.2}$, respectively. These capacitors are adjusted to reduce the ringing of $I_{sub.1}$ and $I_{sub.2}$. The drain of MOSFET $M_{sub.1}$ or $M_{sub.2}$ is connected to current adder 320. According to Mulder et al., the current $I_{sub.x}$ through $C_{sub.x}$ is equal to $\frac{V_{sub.T}}{V_{sub.T} + I_{sub.Q}}$ where $V_{sub.T}$ is the bipolar transistor thermal voltage. From equation (2), $I_{sub.Q} = I_{sub.2} - I_{sub.1}$, and the only difference between the two subcircuits is the current $I_{sub.x}$. As realized, current-mode circuit 300 also compensates for finite beta effect.

Detailed Description Text (6):

Referring to FIGS. 4 and 2A, the loss control loop circuit of FIG. 2A can be

modified to include current-mode circuit 300 of FIG. 3A. An envelope detector 420 replaces rectifier 220, circuit 240 is replaced by low-pass, high DC gain filter 440, and current-mode circuit 300 is placed between envelope detector 420 and low-pass filter 440. The resulting loss control loop circuit controls Q, and thus equivalently controls the function Q but it does not control $V_{sub.ENV}$ itself. When the loop in FIG. 4 makes Q infinite, Equation (2) shows that Q is independent of the value of $V_{sub.ENV}$ (assuming $V_{sub.ENV} \neq 0$). Thus the value of $V_{sub.ENV}$ is not controllable using the circuit of FIG. 4.

Detailed Description Text (7):

In order to control $V_{sub.ENV}$, the loop circuit of FIG. 4 can be modified as shown in FIG. 5. An amplitude regulator 500 can be placed in parallel with current-mode circuit 300 of FIG. 3A, i.e. between envelope detector 420 and low-pass, high DC gain filter 440. A preferred embodiment is shown in FIG. 6A, in which amplitude regulator 500 consists of a voltage difference detector 510 and a charge pump 520. Voltage difference detector 510 includes two comparators 514, 518, arranged to output "up" and "down" signals U, D to charge pump 520, which includes two DC current sources $I_{sub.3}$, $I_{sub.4}$ and two CMOS switches $S_{sub.1}$, $S_{sub.2}$. Each CMOS switch $S_{sub.1}$, $S_{sub.2}$ includes an n-channel MOSFET, into which the U or D signal is provided, and a p-channel MOSFET, into which the inverse U or D signal is provided. One type of charge pump 520 is pictured in FIG. 6B. In that figure, current source $I_{sub.3}$ is made of two PNP bipolar transistors $Q_{sub.7}$, $Q_{sub.8}$ connected in series between $V_{sub.dd}$ and switch $S_{sub.1}$. Analogously, current source $I_{sub.4}$ is made of two NPN bipolar transistors $Q_{sub.9}$, $Q_{sub.10}$ connected in series between switch $S_{sub.2}$ and ground. The bases of the four bipolar transistors $Q_{sub.7}$, $Q_{sub.8}$, $Q_{sub.9}$, $Q_{sub.10}$ of the charge pump shown in FIG. 6B are controlled by four bias voltages $V_{sub.bias\ p3}$, $V_{sub.bias\ p4}$, $V_{sub.bias\ n3}$, $V_{sub.bias\ n4}$, whose values are chosen based on the values chosen for $I_{sub.3}$ and $I_{sub.4}$, as will be shown later. In order to have high DC gain, low-pass filter 440 can be realized as an integrator, which ideally has infinite gain at DC. A simple, one-pole integrator is shown in FIGS. 6A and 6B as an integrating capacitor, $C_{sub.INT}$. When Q is infinite, making $I_{sub.Q} = 0$, if $V_{sub.REF} > V_{sub.ENV}$, the output U of comparator 514 goes high sending a signal to charge pump 520 to connect $I_{sub.3}$ to the output of amplitude regulator 500, which charges $C_{sub.INT}$, increasing $V_{sub.CON}$. This increases $G_{sub.N}$, thus increasing $V_{sub.ENV}$, as seen in the latter part of Equation (1). Conversely, if $V_{sub.REF} < V_{sub.ENV}$, the output D of comparator 518 goes high sending a signal to charge pump 520 to connect $I_{sub.4}$ to the output of amplitude regulator 500, which discharges $C_{sub.INT}$, decreasing $V_{sub.CON}$ and decreasing $G_{sub.N}$, thus decreasing $V_{sub.ENV}$.

Detailed Description Text (10):

The present invention is preferably used in circuits that operate in the GHz range, rather than the low-MHz range described above. In this region, the circuits of FIGS. 8A-8C can be used. FIGS. 8A and 8B are schematic diagrams of examples of negative conductance circuits 260 that may be used in a high-frequency embodiment of the present invention. Many different negative conductance circuits that can be used at high frequencies will be known to those skilled in the art. The choice of the actual components is based on the technology used and the parasitics associated with the technology. The structure of the negative conductance circuit is not as important for choosing loop design parameters as the relationship between $G_{sub.N}$ and $V_{sub.CON}$. The circuit of FIG. 8A is similar to negative conductance circuit 260 (FIG. 2B), but has been modified to achieve better performance and to include biasing. The circuit of FIG. 8B is another example of a negative conductance circuit designed with only resistors and NPN bipolar transistors. FIG. 8C is a schematic diagram of an example of a charge pump 520 that may be used in a high-frequency embodiment of the present invention. As with the charge pump in FIG. 6B, this charge pump uses the both the up and down signals from voltage difference detector 510 as well as the inverse up and down signals.

Detailed Description Text (16):

The response of the system operated in the preferred frequency range yields similar results as those shown in FIG. 7, with controlled $V_{sub.CON}$ and output VCO voltage. The only difference is that the fundamental frequency of the control voltage, $V_{sub.CON}$, is approximately three orders of magnitude faster than that shown in FIG. 7, i.e. approximately 5-10 MHz. The prior art circuit, which was not able to operate

on a breadboard at 3 MHz, is also not able to operate at 1.8 GHz.

CLAIMS:

1. A loss control loop circuit for controlling the amplitude of the output voltage of a voltage-controlled oscillator (VCO), said VCO output voltage being controlled by a VCO control voltage, said circuit comprising:

an envelope detector coupled to receive said VCO output voltage and providing a VCO output envelope voltage;

an amplitude regulator coupled to receive said VCO output envelope voltage and a reference voltage, said amplitude regulator providing a sourcing current if said VCO output envelope voltage is less than said reference voltage, and drawing a sinking current if said VCO output envelope voltage is greater than said reference voltage;

a current-mode circuit coupled to receive said VCO output envelope voltage and providing a control current;

a low-pass filter having high DC gain for integrating said control current and said sourcing or sinking current from said amplitude regulator to provide said VCO control voltage to the VCO; and

means for providing said VCO control voltage to the VCO.

6. The circuit according to claim 1, wherein said amplitude regulator comprises:

a voltage difference detector coupled to receive said VCO output envelope voltage and said reference voltage, said voltage difference detector providing an up signal if said VCO output envelope voltage is less than said reference voltage, and providing a down signal if said VCO output envelope voltage is greater than said reference voltage; and

a charge pump coupled to receive said up and down signals and providing said sourcing current if said up signal is high and drawing said sinking current if said down signal is high.

7. The circuit according to claim 6, wherein said voltage difference detector comprises:

first and second comparators each being coupled to receive said VCO output envelope voltage and said reference voltage,

said first comparator being responsive to said VCO output envelope voltage being less than said reference voltage for providing said high up signal to the output of said voltage difference detector, and

said second comparator being responsive to said VCO output envelope voltage being greater than said reference voltage for providing said high down signal to the output of said voltage difference detector.

10. A loss control loop circuit for stabilizing the amplitude of the output voltage of a voltage-controlled oscillator (VCO), said VCO output voltage being controlled by a VCO control voltage, said circuit comprising:

an envelope detector coupled to receive said VCO output voltage and providing a VCO output envelope voltage;

a current-mode circuit coupled to receive said VCO output envelope voltage and providing a control current;

a low-pass filter having high DC gain for integrating said control current to provide said VCO control voltage to the VCO; and

means for providing said VCO control voltage to the VCO.

12. A master-slave filter tuning system comprising:

a tuned filter coupled to receive an input voltage, a frequency control signal, and a Q-control signal, and providing a filtered output voltage;

a frequency control circuit providing said tuned filter frequency control signal;

a Q-control circuit providing said tuned filter Q-control signal; and

a voltage-controlled oscillator (VCO) coupled to receive said tuned filter frequency control signal and said tuned filter Q-control signal and providing a VCO output voltage,

wherein said Q-control circuit comprises:

an envelope detector coupled to receive said VCO output voltage and providing a VCO output envelope voltage;

an amplitude regulator coupled to receive said VCO output envelope voltage and a reference voltage, said amplitude regulator providing a sourcing current if said VCO output envelope voltage is less than said reference voltage, and drawing a sinking current if said VCO output envelope voltage is greater than said reference voltage;

a current-mode circuit coupled to receive said VCO output envelope voltage and providing a control current; and

a low-pass filter having high DC gain for integrating said control current from said current-mode circuit and said sourcing or sinking current from said amplitude regulator to provide said VCO control voltage to the VCO.

Search Results - Record(s) 1 through 1 of 1 returned.**1. Document ID: US 4159448 A**

L34: Entry 1 of 1

File: USPT

Jun 26, 1979

DOCUMENT-IDENTIFIER: US 4159448 A

TITLE: Communication systems

US Patent No. (1):
4159448Detailed Description Text (35):

The double balanced modulator 100 will operate either as a modulator or as a phase detector. Here, it is used as the latter. It is entirely conventional and is shown as a block in FIG. 4 for simplicity. The remainder of this circuit is embraced by but does not limit the invention. Transistors 104, 106, and 108 are arranged so that the bias to which they are subjected depends upon the relative values of resistors 118, 120, and 122. Current in those three transistors will increase and decrease with source voltage, but the relative values of the current will remain unchanged. That is important because the collectors of transistors 104, 106, and 108 are connected to pins 5, 6, and 12, respectively, of the phase detector. The current at pin 6 and the current at pin 12 are equal to one another, and to the current entering at pin 5 when the input signal to the phase detector is zero. When an intermediate frequency signal is applied at the input terminals 1 and 10 of the phase detector, the current entering at pins 6 and 12 will change. One will increase and the other will decrease, and the amount of that increase and decrease is a function of the amplitude of the difference in the voltages applied to input terminals 1 and 10. While the inputs are derived from the same source, the intermediate frequency signal of the receiver, that signal is applied to one terminal through a limiter. It is applied directly to the other terminal so the effective voltage input to the phase detector is the amount by which the direct signal exceeds the limited signal. There can be a difference only when there is a signal. Therefore, the phase detector 100 provides an output at its terminals 6 and 12 when there is a burst of intermediate frequency energy at the input, and it provides zero output when there is no intermediate frequency signal input. Consequently, an output will appear at terminals 6 and 12 each time that a pulse of energy is received from the transmitting station, and the signal will begin at the time of beginning of the input pulse and it will end at the time of ending of that input pulse.

CLS-1 REF-1 SEQ-1 ATT-1 

| Terms | Documents |
|-------------|-----------|
| l28 and L33 | 1 |

Display Format:

KWIC

Change Format

Previous Page

Next Page